

IN THE SPECIFICATION:

Please replace the paragraph on page 4, starting at line 5 with the following text:

B1  
The memory cell according to the present invention, the edge of the source region on the side of the channel region is defined by the side wall insulating layer of the control gate, and the edge of the drain region on the side of the channel region is defined by the edge of the control gate or by the outer side of the thin side wall insulating layer or the side surface of the control gate. Accordingly, there is obtained an asymmetric memory cell structure, in which the overlap of the source region with the electric charge accumulating portion (typified by the floating gate) is set to the minimum necessary enough to cause no offset, and the overlap of the drain region with the floating gate is set larger than that of the source region. It is therefore possible to reduce a gate length while ensuring an effective channel length required.

Please replace the paragraph on page 9, starting at line 26 with the following text:

B2  
Thereafter, an oxide layer 13 is provided on exposed surfaces of the control gate 6 and of floating gate 4 and on the surface of the substrate 1 by effecting the thermal oxidation. As shown in FIG. 2C, a resist pattern 11 covering an area on the source region side is thereafter provided by the lithography process. Then, the ion, i.e., arsenic is implanted, thereby providing the  $n^+$  type drain region 9 self-aligned with the control gate 6. At this stage, however, the impurity in the drain region 9 is not yet activated. The dose quantity of arsenic is set on the order of, e.g.,  $2 \times 10^{15}/\text{cm}^2$ .

Please replace the paragraph on page 10, starting at line 4 with the following text:

B3  
Next, the lithography process is again executed, thereby providing a resist pattern 12 covering an area on the side of the drain region 9 as shown in FIG. 2E. Then, the ion, i.e., arsenic, is implanted, thereby providing the  $n^+$  type source region 8 self-aligned with the side wall insulating layer 7. At that time the dose quantity of arsenic is set on the order of, e.g.,  $5 \times 10^{15}/\text{cm}^2$ .

Please replace the paragraph on page 15, starting at line 3 with the following text: